AMENDMENTS TO THE CLAIMS:

Claims 1-150 (previously canceled)

1. (previously presented) A controller device for controlling a synchronous dynamic random access memory device, the controller device comprises:

first output driver circuitry to output block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device; and

input receiver circuitry to receive the amount of data output by the memory device.

2. (currently amended) The controller device of claim 1 further including second output driver circuitry to output an operation code to the memory device, wherein the operation code specifies a read operation, and wherein, in response to the operation code, the memory device outputs the amount of data.

3. (previously presented) The controller device of claim 2 wherein the operation code is included in a packet.

4. (currently amended) The controller device of claim 3 wherein the block size information and the operation code are included in the same packet.

155. (currently amended) The controller device of claim 152 wherein the first output driver circuitry outputs the block size information in response to a first transition of an external clock signal, and the second output driver circuitry outputs the operation code in response to a second transition of the external clock signal.

156. (previously presented) The controller device of claim 152 wherein the first output driver circuitry and the second output driver circuitry output address information to the memory device.

157. (previously presented) The controller device of claim 156 wherein the block size information, the address information and the operation code are output to the memory device via an external bus.

158. (previously presented) The controller device of claim 157 wherein the external bus includes a plurality of signal lines to carry, in a multiplexed format, the block size information, the operation code and the address information.

159. (previously presented) The controller device of claim 151 further including delay locked loop circuitry, coupled to the input receiver circuitry, to generate an internal clock signal, wherein the input receiver circuitry samples the amount of data in response to the internal clock signal.

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~~160~~. (currently amended) The controller device of claim ~~151~~ further including delay locked loop circuitry, coupled to the first output driver circuitry, to generate an internal clock signal, wherein the first output driver circuitry outputs the block size information ~~in response~~ synchronously with respect to the internal clock signal.

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~~161~~. (previously presented) The controller device of claim ~~151~~ wherein the block size information is a binary code.

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~~162~~. (currently amended) The controller device of claim ~~151~~ wherein the input receiver circuitry samples:

a first portion of the amount of data during a first half of a clock cycle of ~~the~~ an external clock signal; and

a second portion of the amount of data during a second half of the clock cycle of the external clock signal.

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~~163~~. (currently amended) The controller device of claim ~~151~~ wherein the input receiver circuitry samples:

a first portion of the amount of data in response to a rising edge of ~~the~~ an external clock signal; and

a second portion of the amount of data in response to a falling edge of the external clock signal.

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~~164~~. (previously presented) An integrated circuit device comprising:

a plurality of output drivers to output block size information to a second integrated circuit device, wherein the block size information represents an amount of data to be output by the second integrated circuit device;

a delay locked loop to generate an internal clock signal; and

a plurality of input receivers, coupled to the delay locked loop, to sample the amount of data output by the second integrated circuit device, wherein the amount of data is sampled synchronously with respect to the internal clock signal.

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~~165~~. (currently amended) The integrated circuit device of claim 17 ~~164~~ further including a clock receiver to receive an external clock signal, wherein the delay locked loop generates the internal clock signal using the external clock signal.

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~~166~~. (currently amended) The integrated circuit device of claim 17 ~~164~~ wherein the plurality of output drivers outputs the block size information to the second integrated circuit device via a bus, wherein the bus includes a plurality of signal lines.

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~~167~~. (currently amended) The integrated circuit device of claim 19 ~~166~~ wherein the plurality of signal lines ~~carry~~ carries, in a multiplexed format, an operation code, address information and the block size information.

~~168~~. (previously presented) The integrated circuit device of claim ~~164~~ wherein the block size information is a binary code.

~~169~~. (previously presented) The integrated circuit device of claim ~~164~~ wherein the block size information is included in a request packet.

~~170~~. (previously presented) The integrated circuit device of claim ~~169~~ wherein the amount of data output by the second integrated circuit device is included in a data packet.

~~171~~. (currently amended) The integrated circuit device of claim ~~170~~ wherein the data packet is output by the second integrated circuit device onto a set of signal lines, and the request packet is output to the second integrated circuit device via the ~~same~~ set of signal lines.

~~172~~. (currently amended) The integrated circuit device of claim ~~164~~ wherein:

during a first half of a clock cycle of ~~the~~ an external clock signal, the plurality of input receivers samples a first portion of the amount of data output by the second integrated circuit device; and

during a second half of the clock cycle of the external clock signal, the plurality of input receivers samples a second portion of the amount of data output by the second integrated circuit device.

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~~173~~. (currently amended) The integrated circuit device of claim ~~164~~ 17 wherein:

the plurality of input receivers samples a first portion of the amount of data output by the second integrated circuit device in response to a rising edge of ~~the~~ an external clock signal; and

the plurality of input receivers samples a second portion of the amount of data output by the second integrated circuit device in response to a falling edge of the external clock signal.

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~~174~~. (currently amended) An integrated circuit device for controlling a synchronous memory device, the ~~controller~~ integrated circuit device comprises:

clock receiver circuitry to receive an external clock signal;

delay locked loop circuitry, coupled to the clock receiver circuitry, to generate an internal clock signal; and

a first plurality of output drivers, coupled to the delay locked loop circuitry, to output an amount of write data ~~in response~~ synchronously with respect to the internal clock signal.

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~~175~~. (currently amended) The integrated circuit device of claim 28 ~~174~~ further including input receivers to sample read data that is output by the synchronous memory device.

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~~176~~. (currently amended) The integrated circuit device of claim 29 ~~175~~ wherein the input receivers are coupled to the delay locked loop circuitry to sample the read data ~~in response~~ synchronously with respect to the internal clock signal.

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~~177~~. (currently amended) The integrated circuit device of claim ~~174~~ 29 ~~173~~ wherein:

synchronously with respect to ~~on~~ a rising edge transition of the external clock signal, the input receivers sample a first portion of the read data ~~that is output by the memory device~~; and

synchronously with respect to ~~on~~ a falling edge transition of the external clock signal, the input receivers sample a second portion of the read data ~~that is output by the memory device~~.

32 ~~178~~. (currently amended) The integrated circuit device of claim 28 ~~174~~ further including a second plurality of output drivers to output ~~a first~~ an operation code to the synchronous memory device, wherein the ~~first~~ operation code specifies a read operation, ~~and~~ wherein the synchronous memory device, in response to the ~~first~~ operation code, outputs read data.

33 ~~179~~. (currently amended) The integrated circuit device of claim 28 ~~174~~ wherein:

the first plurality of output drivers outputs a first portion of the amount of write data in response to a rising edge transition of the external clock signal; and

the first plurality of output drivers outputs a second portion of the amount of write data in response to a falling edge transition of the external clock signal.

34 ~~180~~. (currently amended) The integrated circuit device of claim 28 ~~174~~ further including a second plurality of output drivers to output ~~a second~~ an operation code to the synchronous memory device, wherein the ~~second~~ operation code specifies a write operation, and wherein the memory device, in response to the second operation code, samples the amount of write data.

35 ~~180~~. (currently amended) The integrated circuit device of claim 28 ~~174~~ wherein the first plurality of output drivers are coupled to the synchronous memory device via an external bus that includes

a plurality of signal lines.

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~~102~~. (currently amended) The integrated circuit device of claim ~~101~~ 35 wherein the first plurality of output drivers outputs an operation code and address information to the synchronous memory device, in a multiplexed format, via the plurality of signal lines.

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~~103~~. (currently amended) The integrated circuit device of claim ~~101~~ 26 wherein the first plurality of output drivers includes a plurality of output drivers to output an operation code to the synchronous memory device, wherein the operation code specifies a read operation, and wherein the memory device outputs read data in response to the operation code ~~specifying the read operation~~.

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~~184~~. (previously presented) An integrated circuit controller device for controlling a synchronous dynamic random access memory device, the controller device comprises:

a first plurality of output drivers to output block size information to the memory device, wherein the block size information represents an amount of data to be output by the memory device;

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a second plurality of output drivers to output an operation code to the memory device, wherein the operation code specifies a read operation, and wherein the memory device outputs the amount of data to the controller device in response to the operation code; and

a plurality of input receivers to receive the amount of data output by the memory device.

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~~185~~. (previously presented) The controller device of claim 38 ~~184~~ wherein the operation code is included in a packet.

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~~186~~. (currently amended) The controller device of claim 39 ~~185~~ wherein the block size information and the operation code are included in the ~~same~~ packet.

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~~187~~. (previously presented) The controller device of claim 38 ~~184~~ wherein the block size information is output in response to a first transition of an external clock signal and the operation code is output in response to a second transition of the external clock signal.

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~~188~~. (previously presented) The controller device of claim ~~184~~ wherein both the first plurality of output drivers and the second plurality of output drivers output address information to the memory device.

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~~189~~. (previously presented) The controller device of claim ~~188~~ wherein the block size information, the operation code, and the address information are output, in a multiplexed format, to the memory device via an external bus.

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~~190~~. (previously presented) The controller device of claim ~~184~~ further including a clock receiver to receive an external clock signal, wherein the first plurality of output drivers outputs the block size information synchronously with respect to the external clock signal.

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~~191~~. (currently amended) The controller device of claim ~~190~~ further including a delay locked loop coupled to the clock receiver and the plurality of input receivers, wherein the delay locked loop generates an internal clock signal, and wherein the plurality of input receivers samples the amount of data in response to the internal clock signal.

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~~192~~. (currently amended) The controller device of claim ~~190~~ further including a delay locked loop coupled to the first plurality of output drivers and the clock receiver, wherein the delay locked loop generates an internal clock signal, and wherein the first plurality of output drivers ~~circuitry~~ outputs the block

size information in response to the internal clock signal.

~~193~~. (previously presented) The controller device of claim ~~184~~ wherein the block size information is a binary code.

~~194~~. (currently amended) The controller device of claim ~~184~~ further including a clock receiver to receive an external clock signal, wherein:

the plurality of input receivers samples a first portion of the amount of data during a first half of a clock cycle of the external clock signal; and

the plurality of input receivers samples a second portion of the amount of data during a second half of the clock cycle of the external clock signal.

~~195~~. (New) The controller device of claim ~~184~~ wherein, during a clock cycle of ~~the~~ external clock signal, the plurality of input receivers samples two bits of data of the amount of data output by the memory device via an external signal line.

~~196~~. (New) The controller device of claim ~~151~~ further including a clock receiver to receive an external clock signal, wherein, during a clock cycle of an external clock signal, the input receiver receives two bits of data from an external signal line, wherein the two bits of data are included in the amount of data output by the memory device.

~~197~~ 41. (New) The controller device of claim ~~160~~ 10 wherein the delay locked loop circuitry includes at least one variable delay line used in the generation of the internal clock signal.

~~198~~ 12. (New) The controller device of claim ~~197~~ 11 wherein the delay locked loop circuitry includes more than one variable delay line used in the generation of the internal clock signal.

~~199~~ 21. (New) The controller device of claim ~~164~~ 17 further including a clock receiver to receive an external clock signal, wherein, during a clock cycle of the external clock signal, the plurality of input receivers samples two bits of data from an external signal line, wherein the two bits of data are included in the amount of data.